IN THE CLAIMS:

1. (Currently amended) A circuit arrangement comprising a multi-wire line for supplying current to, and for emitting electric signals from a sensor, the electric signals corresponding to measured values to an evaluation module via a signal line, characterized in that, for eliminating measuring errors caused by short circuits, first and second resistors ~~(7,8)~~ with voltage tap-off at the second resistor ~~(8)~~ and a transistor ~~(9)~~ connected to a clock-pulse generator ~~(10)~~ and bridging the first resistor in a clocked manner are connected in series to the signal line, and in that a comparator ~~(17)~~ is provided downstream from the resistors ~~(7,8)~~ to compare the values received via the second resistor ~~(8)~~ in subsequent switching positions of the transistor and for issuing a short-circuit error message to the evaluation module ~~(3)~~ if measured values in subsequent clock pulses differ.

2. (Currently amended) The circuit arrangement according to claim 1, characterized in that first and second electronic switches ~~(11, 12)~~ are provided downstream from the resistors ~~(7, 8)~~ that, in sync with the pulses from the clock pulse generator ~~(10)~~, alternately provide a conducting connection to a first or second storage module, respectively, ~~such as buffer condenser (13, 14),~~ for temporary storage of the measured values tapped off the second ~~transistor (8)~~ resistor in the respective clock pulse ~~(t1 or t2)~~ with the transistor ~~(9)~~ closed or open.

3. (Currently amended) The circuit arrangement according to ~~claims 1 or 2~~ claim 1, characterized in that a voltage divider with voltage-dividing resistors ~~(15, 16)~~ is provided upstream of the comparator.

4. (Cancelled)

5. (New) The circuit arrangement according to claim 2, characterized in that a voltage divider with voltage-dividing resistors is provided upstream of the comparator.

6. (New) The circuit arrangement according to claim 2, characterized in that the first or second storage module is a buffer condenser.

7. (New) The circuit arrangement according to claim 1, characterized in that a data buffer for temporary storage of the measuring signal emitted by the sensor and for feeding it to the evaluation module if the measurement was free of short circuits is provided upstream of the comparator.

8. (New) The circuit arrangement according to claim 2, characterized in that a data buffer for temporary storage of the measuring signal emitted by the sensor and for feeding it to the evaluation module if the measurement was free of short circuits is provided upstream of the comparator.

9. (New) The circuit arrangement according to claim 3, characterized in that a data buffer for temporary storage of the measuring signal emitted by the sensor and for feeding it to the evaluation module if the measurement was free of short circuits is provided upstream of the comparator.

10. (New) The circuit arrangement according to claim 5, characterized in that a data buffer for temporary storage of the measuring signal emitted by the sensor and for feeding it to the evaluation module if the measurement was free of short circuits is provided upstream of the comparator.

11. (New) The circuit arrangement according to claim 6, characterized in that a data buffer for temporary storage of the measuring signal emitted by the sensor and for feeding it to the evaluation module if the measurement was free of short circuits is provided upstream of the comparator.